Electronic Version
Stylesheet Version v1.1.1

[THIN FILM TRANSISTOR AND PIXEL STRUCTURE THEREOF]

Abstract

A thin film transistor and a pixel structure with the same are disclosed. The thin film transistor includes a gate electrode with at least one notch, a gate dielectric layer, a source region, a drain region, and a channel layer. The gate electrode is on a substrate. The gate dielectric layer is on the substrate and covers the gate electrode. The source region is on the gate dielectric layer, wherein it is over a region outside the notch of the gate electrode and overlaps a portion of the gate electrode. The drain region is on the gate dielectric layer, wherein it is over the notch of the gate electrode and overlaps the gate electrode at the edge of the notch. Further, the channel layer is on the gate dielectric layer and between the source and drain regions. Due to asymmetric design of the source and drain regions, the parasitic capacitance change can be substantially reduced when a misalignment of the upper and lower metal layers occurs.